## REMARKS/ARGUMENTS

Applicants received the final Office action dated August 10, 2006, in which the Examiner: 1) rejected claims 1-3, 5, 8-11, 14, 17 and 19 under 35 U.S.C. § 102(b) as anticipated by Walker; 2) rejected claim 18 as obvious over Walker in view of Erickson; 3) rejected claims 4 and 12 as obvious over Walker in view of McKenzie; 4) rejected claims 6 and 13 as obvious over Walker in view of Piccirillo; and 5) rejected claims 7 and 16 as obvious over Walker in view of Nakamura. With this Response, Applicants claim 1. Based on the amendment and arguments contained herein, Applicants believe all pending claims to be in condition for allowance.

Walker teaches a memory subsystem that comprises a mechanism (error correction codes) that enables bit errors to be detected and corrected. The error correction mechanism functions upon performing a read operation. See e.g., page 4, paragraph [0045]. In performing error correction during a read operation, error correction is only performed on data that is read—other areas of memory not being read are not tested for errors and thus "areas of memory may sit idle for extended periods thereby allowing data errors to accumulate undetected." Paragraph [0046].

Walker's contribution is, at least in part, a "cleansing operation" that "relies on the normal ECC and error logging mechanisms to validate the health of the memory sub-system 40." The cleansing procedure is further detailed in paragraphs [0047]-[0048]. These paragraphs explain that cleansing logic 70 issues its own read commands that are arbitrated along with normal read and write commands. By issuing read commands, the cleansing logic 70 essentially forces a read of memory for the purpose of checking for errors, since error checking occurs during reads. This is what paragraph [0040] means when it states that the cleansing procedure "relies on the normal ECC and error logging mechanisms." The "normal ECC and error logging mechanisms" are the mechanisms that occur during a normal read of memory. Thus, the error detection mechanism of Walker necessarily functions while the memory modules being tested are fully operational and otherwise being used to perform normal

read and write operations. The testing process described in paragraphs [0047-0048] of Walker does not test an isolated memory module, but rather tests a memory module that can receive and react to read requests. Walker also discloses memory modules in paragraph [0029] that operate in a RAID configuration. Nowhere, however, does Walker disclose testing of a RAID memory module that is tested while isolated.

The final Office action of August 10, 2006, noted that claim 1 requires that a memory module may be isolated and, while isolated, the memory module "can be" tested. The Office action states that "[w]hile the particular failed memory [of Walker] is removed/isolated, all of the transactions that target the isolated memory module can be completed without loss of data since the other four memory modules are working under a RAID scheme, and while the failed memory module is isolated, it **can be tested**." Page 11 (emphasis in original).

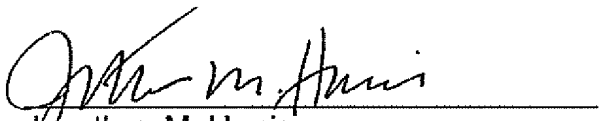
Applicants have amended claim 1 to clarify what is meant by an "isolated" memory module. Claim 1 now requires that a "memory module is present in the computer system but isolated wherein transactions that target said isolated memory module can complete without loss of data and without accessing said isolated memory module." Thus, an isolated memory module is a memory module that is present in the system. This limitation excludes memory modules that have been removed from the system. Moreover, claim 1 requires testing of a memory module that, while present in the system, is nevertheless isolated. This is in contrast to the Examiner's statement regarding Walker that "while the particular failed memory is removed/isolated...it can be tested." No other art of record satisfies this deficiency of Walker. For at least this reason, claim 1 and all claims dependent thereon are allowable over the cited art.

The remaining independent claims, and their dependent claims, are allowable for the same or similar reasons as claim 1.

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of

time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,



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